SWITCHING ANALYSIS

Testing for reliability in power converter designs

White paper | Version 02.00 | Marcus Sonst

ROHDE&SCHWARZ

Make ideas real

CONTENTS

1 Introduction 3

2 Probing 3
2.1 Selecting the right current and voltage probe 3
2.2 Different floating measurement techniques and their considerations 4
2.3 The relationship between bandwidth, rise time and slew rate 5
2.4 The influence of accessories on measurements 6
2.5 The importance of the CMRR of the probe 8
2.6 How to properly connect to a converter 8

3 Switching analysis 10
3.1 Parameters used to characterize switching behavior 10
3.2 An example of switching analysis 10

4 Testing for reliability 12
4.1 Trigger on a specific dead time 12
4.2 Trigger on high side V_{GS} glitch for no load 14
4.3 Trigger on high side V_{GS} glitch for high load 15

5 Conclusion 17

1 INTRODUCTION

Testing for reliability in power converter designs can be a stringent process that requires thorough analysis. This is particularly true in safety-related systems in automotive applications or aerospace and defense. There are dynamic factors to consider when testing power converters. The testing process must account for components used in converters and inverters that have operation-point-dependent specifications. A good example of this is the changing DC-bias characteristic of multilayer ceramic capacitors (MLCCs) where the capacitance decreases as applied DC voltage increases. Resonances are also load-dependent, as the current-dependent capacity of a body diode demonstrates.

Component specifications also shift as a result of aging and temperature increases. Ultimately, the key to reliability testing is high test coverage to ensure that power converters are characterized under all types of load and environmental conditions, while also accounting for transient behavior. This article dives into reliability testing of power converters by delving into the basics of probing, basic and advanced switching analysis methods and testing for reliability.

2 PROBING

2.1 Selecting the right current and voltage probe

Current probes take a range of forms:

- Clamp current probes (e.g. R&S®RT-ZC10, R&S®RT-ZC20B, R&S®RT-ZC30)
- Shunt measurements with voltage probe
- Rogowski probes
- LEM and Pearson sensors

Clamp probes, also known as magnetic core current probes, typically measure current consumption of high-speed digital signals, analog signals and power converters. This type of current probe is general-purpose and used for most measurements. Alternatively, a voltage probe can be used in tandem with a sense/shunt resistor to measure voltage drop across the resistor which can, in turn, be converted into current. However, this involves a direct connection with the current carrying circuit, causing power dissipation. Rogowski probes are ideally suited to high current measurements up to the thousands of amps such as inrush currents from motors or switching transients in high-powered converters. Pearson current monitors are current transformer (CT) probes that measure current transients or time-varying currents in high voltage applications. Each of these probes comes with its own pros and cons that must be considered before implementation.

Selecting the right voltage probe involves considering the required voltage range and common mode (CM) voltage range. The probe should be chosen based on whether the setup has a ground reference or is floating. The bandwidth requirements must also be considered, as well as precisely how to connect the probe to the circuit. There are typically many obstacles that might prohibit straightforward access, such as heat sinks and larger PCB components. The following section dives into the various test topologies that voltage probes are used in. The type of voltage probe used will depend heavily on the type of test performed.

2.2 Different floating measurement techniques and their considerations

Four commonly used floating measurement techniques are shown in Figure 1.

Figure 1: Different floating measurement techniques

(a) Floating oscilloscope using an isolating transformer, (b) Single-ended probe using the math function on the oscilloscope, (c) Oscilloscope with a high-voltage differential probe, (d) Isolated channel oscilloscope

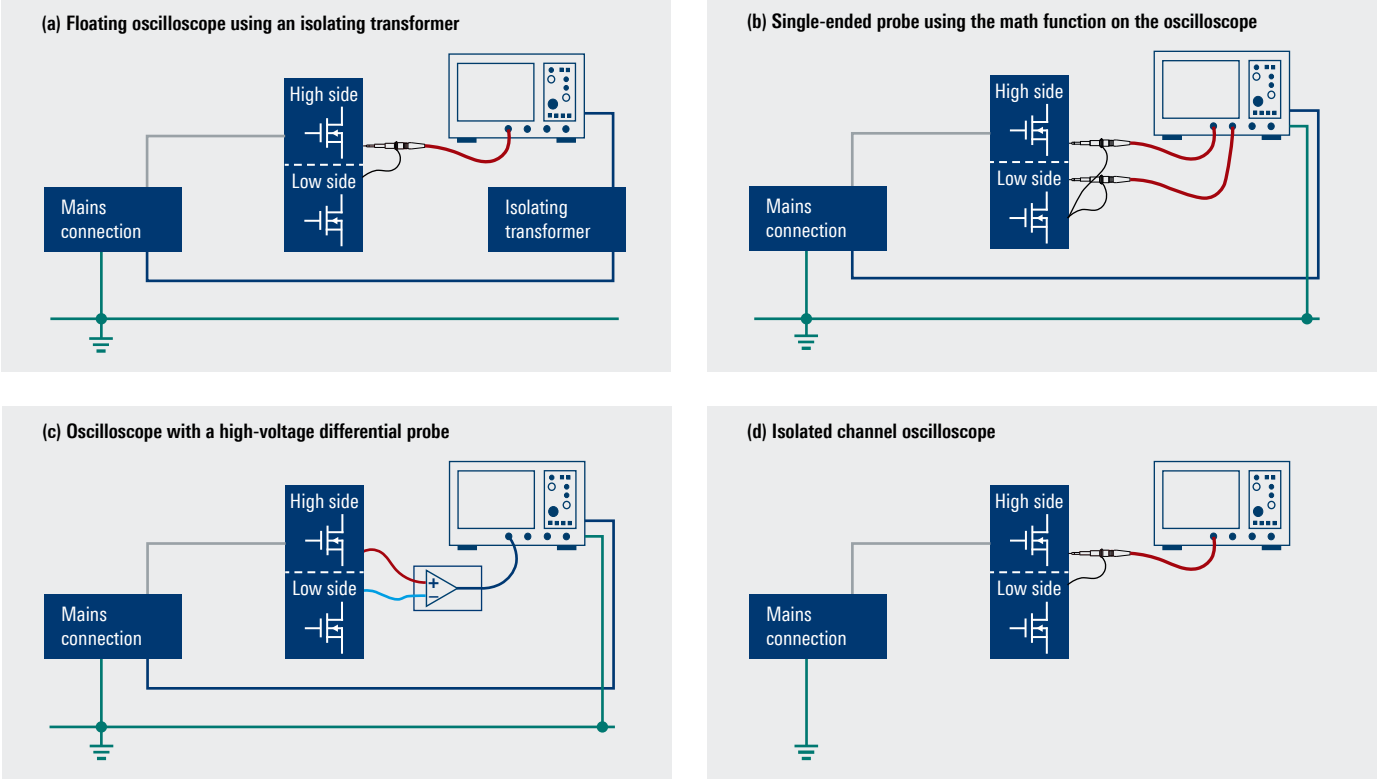


Figure 1(a) includes a mains connection without protective earth (PE), and the driver is connected to the high side (HS) and low side (LS) switch. The oscilloscope is isolated with an isolation transformer, allowing the tester to probe at any point. In this topology, the oscilloscope ground is provided by the device under test (DUT) which may not be 0 V, thereby increasing the risk of electric shock – an unacceptable risk in any case. All grounds are at the same voltage level, which is not necessary. Typically, the BNCs connected to the oscilloscope are grounded, but because an isolation transformer is integrated into the setup, the connectors may no longer be grounded, which means that stray capacitance and inductance of the setup could influence measurements. This test topology is not recommended.

In Figure 1(b), the oscilloscope uses two single-ended probes for a differential channel as well as the oscilloscope's math function, eliminating the need for an isolation transformer. In this setup, the oscilloscope inputs can easily be overdriven and the vertical resolution is limited by the offset range and divider ratio of the probe. The probes must be compensated against each other to achieve good results – a simple skew adjustment is not sufficient, and a complete adjustment over the frequency is needed. In most cases, probes of the same type have to be used; otherwise, compensation is impossible. This setup is also not recommended.

Figure 1(c) shows an oscilloscope with high voltage differential probes, which also eliminates the need for an isolating transformer. With this setup, users can accurately measure small differential voltages in the presence of large common mode voltages up

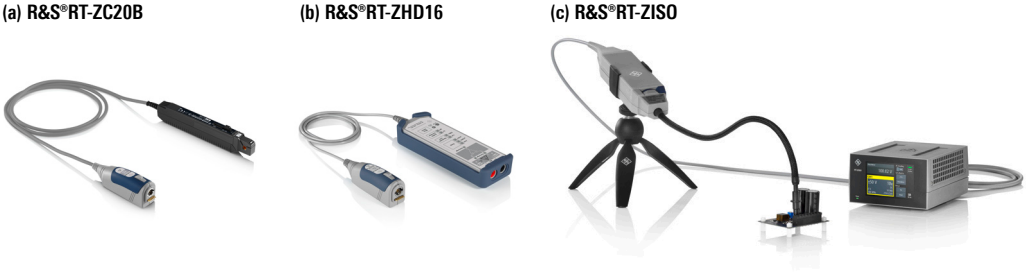
to thousands of volts. There is a high input impedance on the inputs to minimize loading and measurement errors. In this topology, the bandwidth is limited to 200 MHz.

Figure 1(d) uses an isolated oscilloscope, such as the R&S®Scope Rider RTH, with an isolated input that has no direct electrical connector earth ground. The topology has excellent DC gain accuracy and DC measurement accuracy, as well as a low frequency common mode rejection ratio (CMRR) with a bandwidth up to 500 MHz. However, the isolated probes are not truly differential, which may need to be kept in mind during testing. Generally, the topologies shown in Figure 1(c) and Figure 1(d) are recommended.

With newer power electronics technology, components with wide bandgap semiconductors like gallium nitride (GaN) and silicon carbide (SiC) switch at a higher voltage range and even faster edges, with rise and fall times in < 2 ns. This has created a demand for a combination of topologies used in Figure 1(c) and Figure 1(d) to create a new approach to isolated probing. The R&S®RT-ZISO isolated probing system for oscilloscopes is designed to tackle this requirement. It can provide high frequency CMRR and bandwidth up to 1 GHz.

Figure 2: Related Rohde&Schwarz products

(a) R&S®RT-ZC20B current probe, (2) R&S®RT-ZHD16 high voltage probe, (c) R&S®RT-ZISO isolated probing system



2.3 The relationship between bandwidth, rise time and slew rate

The required bandwidth of a test must be estimated when the only known parameter is the rise time (t_r). The rise time is the transition time required for a signal to go from 10% to 90% of the maximum steady state value. The bandwidth (f_{BW}) is the frequency range over which the frequency response of a signal degrades by 3 dB. The correlation between these two parameters can be expressed with Equation 1.

Equation 1:

$$f_{BW} = \frac{0.35}{t_r}$$

This is a useful way to get a quick rough estimate of bandwidth, but it is also an oversimplification. The above equation is derived by considering the response to a first-order passive filter and calculating its step-response in the frequency and time domains. In many cases, however, the response will not mimic that of a passive 1-pole lowpass filter.

The slew rate (SR) identifies the maximum input frequency and amplitude applicable to an amplifier, or large-scale signals. This parameter is directly related to t_r as shown in Equation 2.

Equation 2:

$$SR = \frac{V_{10\ to\ 90}}{t_r}$$

It is easy to identify the peak current of a Miller capacitance by multiplying SR by capacitance (C), two parameters that can be pulled from a data sheet, as shown in Equation 3.

Equation 3:

$$I_{peak} = SR \cdot C$$

Figure 3 shows an example of how rise time and slew rate works on a 1 kV step signal tested with the R&S®RT-ZHD16 high voltage differential probe with a bandwidth of 200 MHz. Measurement results show a t_r of 12 ns and an SR of 61 V/ns. When plugged into Equation 1, this yields a required bandwidth of approximately 30 MHz, a value much lower than the 200 MHz of the probe. This shows that the probe is more than sufficient to adequately measure this signal.

Figure 3: 1 kV step signal testing with the R&S®RT-ZHD16 high voltage differential probe

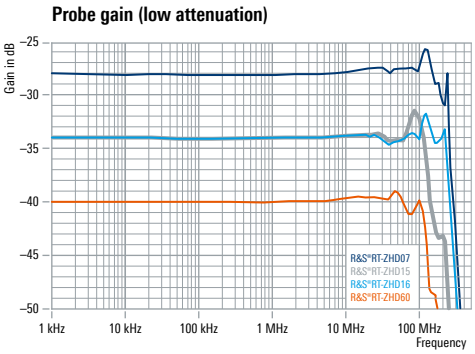
2.4 The influence of accessories on measurements

Because they are an inherent part of the transfer function, cables and clips can have a major influence on measurements, which must be considered when performing reliability testing. A flat transfer function is a key factor in the accuracy of turn-on and turn-off measurements. Moreover, the instability of setups using cabling and clips makes equalization impossible at frequencies higher than 200 MHz.

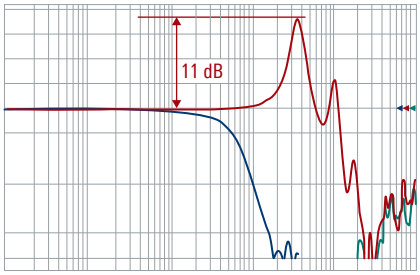
An example of this issue is shown in Figure 4. Figure 4(a) shows the probe gain specified on its data sheet where the response is fairly flat until approximately 100 MHz. When longer leads are used, the response drastically worsens in both the frequency and time domains as seen in Figures 4(b) and 4(c), respectively. In the frequency domain, huge resonances appear that may vary depending on cable length and positioning. In the time domain, high readings with odd switching behavior may appear. Using short leads is recommended, if possible; otherwise, a lowpass filter should be used to obtain more realistic measurements.

Figure 4: Influence of accessories on measurements

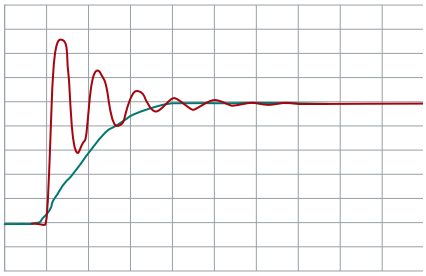
(a) Specified probe gain of different Rohde&Schwarz probes



(b) Frequency domain response of a probe with long leads



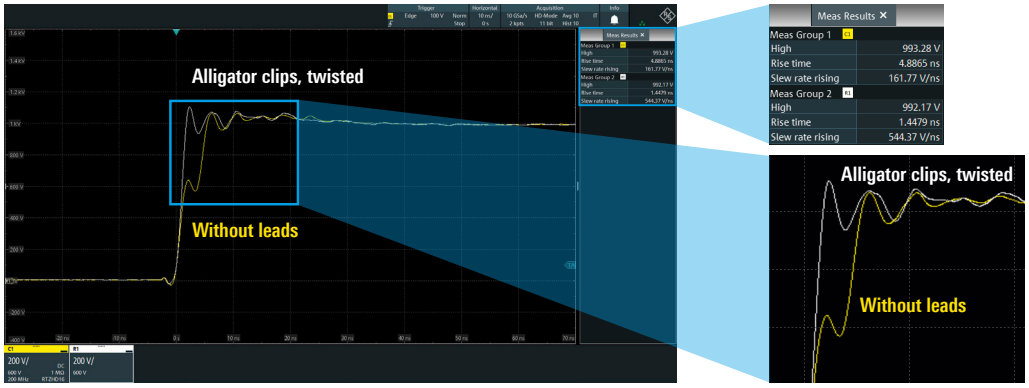
(c) Time domain response of a probe with long leads



The contact method for high voltage probes also matters. Figure 5 shows the impact of using a BNC coaxial cable, a method that does not use leads. The white line shows the measurement results with typical alligator clips, a good response with some ringing. The yellow line shows the results without leads (using a BNC coax). In this case, there is essentially a reflection due to the lack of a proper termination, causing measurement issues. To prevent this effect and obtain more accurate results, leads up to 17 centimeters long should be used because they have the right compensation in the probe head for.

Figure 5: Measurement setup

With alligator clips (white) and with a BNC connected coax (yellow) on the R&S®RT-ZHD probe head



2.5 The importance of the CMRR of the probe

Another factor to consider when probing is the common mode rejection ratio (CMRR) of the probe. The CMRR is a figure of merit that measures a differential amplifier's ability to reject CM signals. CMRR is defined by Equation 4.

Equation 4:

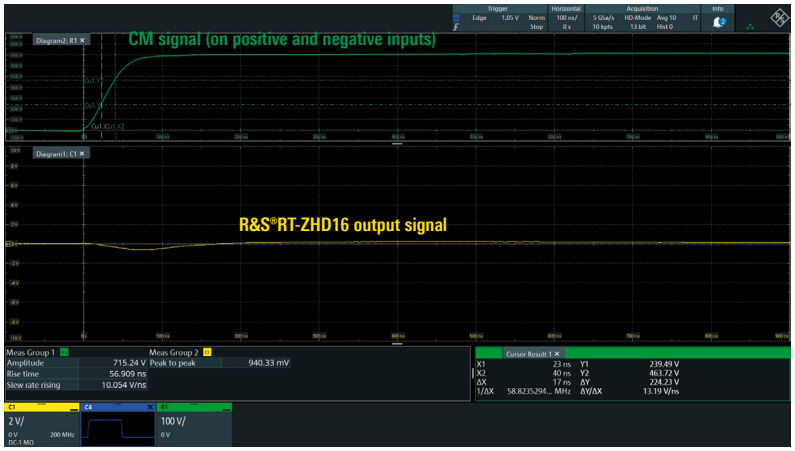
$$CMMR = \frac{Differential\ gain}{Common\ mode\ gain}$$

The differential probe uses the differential amplifier to measure the difference between two signals. However, since differential measurements are made using two different signal paths, they must be as identical as possible in both amplitude response and timing delays in order to provide more accurate measurements. Interconnect path differences such as a high CMRR may distort the measured response.

Since differential measurements are made using two different measurement signal paths, the measurement path amplitude response and timing delays must be closely matched for a high measurement integrity. If the two signal input paths are not carefully matched, interconnect path differences distort the response.

The measured CMRR of the R&S®RT-ZHD16 can be seen in Figure 6. A CM voltage step of 700 V is measured where both inputs are connected to the switch node – similar to the topology in Figure 1(c) – and a rise time of 57 ns is applied, which corresponds to a 6 MHz signal bandwidth. This yields a CMRR of 57 dB, which corresponds to the component's data sheet value (see blue arrow at approx. 6 MHz).

Figure 6: CMRR measurement on the R&S®RT-ZHD16 differential probe

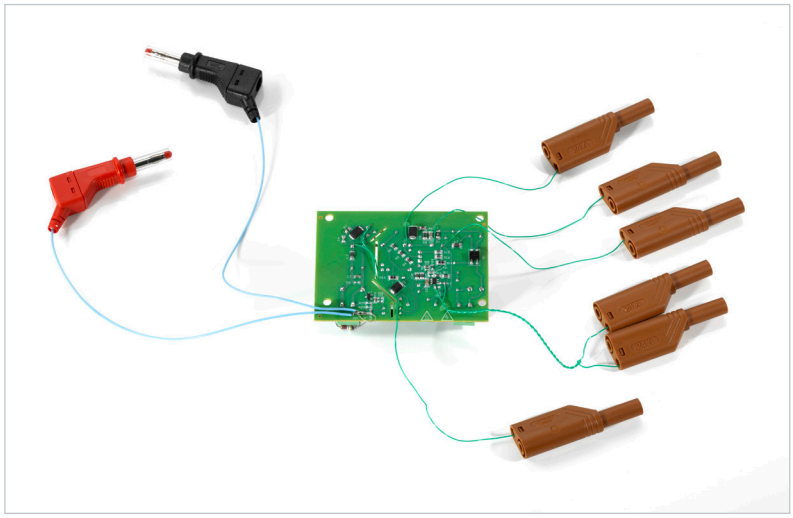


2.6 How to properly connect to a converter

An example of a good connection to a test circuit is shown in Figure 7, where the DUT is a flyback converter evaluation board with a maximum voltage range of 550 V. Six inch Rubadue special cables (T26A01FXXX-2) suitable for up to 1 kV are used with 4 mm connectors that fit well into the R&S®RT-ZHD probe head. Soldered connections are used because they are far more robust than Hirschmann or alligator clip alternatives and exert low mechanical stress on the PCB. This connection also works with sensitive signals such as the sense resistor at the bottom of the PCB, which is tapped with a twisted pair cable for a current controlled mode (CCM) measurement.

Figure 7: A flyback converter evaluation board

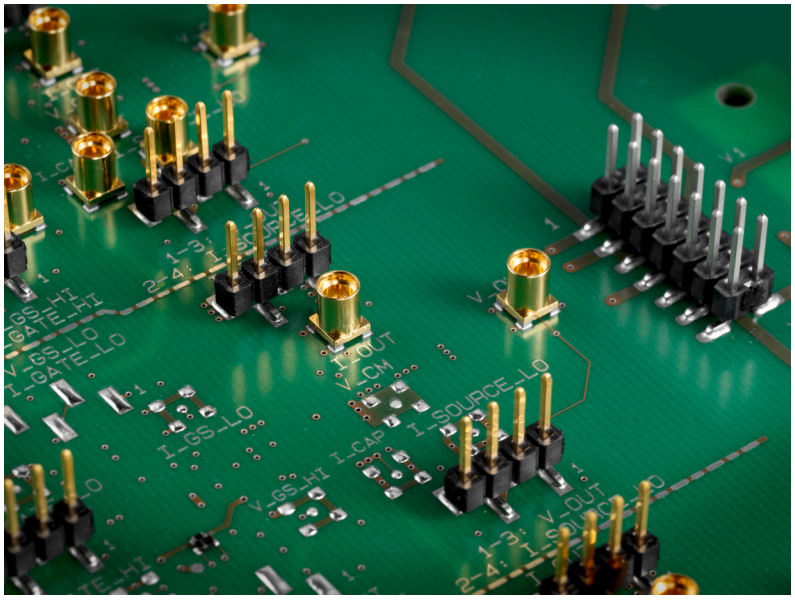
Properly connected to the test equipment for accurate measurements



However, when working with wide bandgap (WBG) semiconductor devices with much faster switching edges, a conventional approach – even with soldered down twisted pair cable – will highly degrade the waveform. Additionally, such connections without a control impedance will cause mismatches and reduce the CMRR of the measurement system. Here, it is necessary to include a coaxial test point (such as MMCX or SMA) in the design to ensure shorter, impedance-matched return paths. The R&S®RT-ZISO isolated probing system for oscilloscopes and the R&S®RT-ZPMMCX passive probe are designed to work with such a coaxial interface and help maintain a high CMRR and noise immunity in such a circuit.

Figure 8: MMCX socket for testing

A new standard to facilitate testing of fast switching and noisy environments



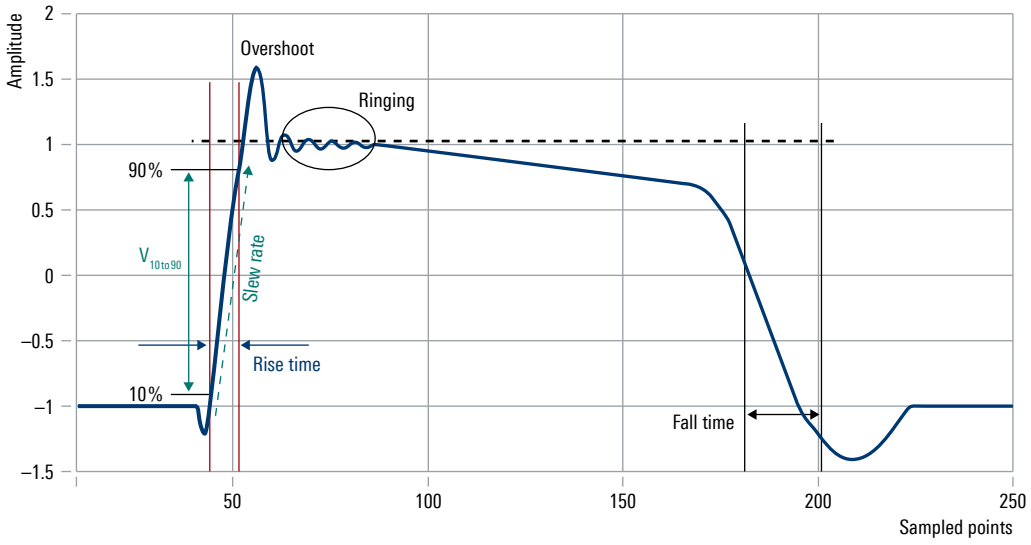
3 SWITCHING ANALYSIS

3.1 Parameters used to characterize switching behavior

The key parameters for characterizing switching are typically rise time/slew rate, overshoot and ringing (Figure 9). Overshoot can be important, for instance, in assessing whether the breakdown voltage of a transistor is exceeded. Ringing is important to assess in many cases, such as testing the effectiveness of a snubber. Assessing rise time, fall time and slew rate is critical, not only because these parameters influence dynamic power dissipation and dead time but also because knowing their values is necessary for gate driver design.

Figure 9: Key parameters in switching analysis

Rise time, fall time, slew rate, overshoot and ringing



3.2 An example of switching analysis

Figure 10 shows an oscilloscope measurement looking at overshoot and maximum voltage to check the safety margin for the drain-source breakdown voltage (BVDSS) of the DUT. The DUT is an application circuit that uses the LM5039 controller/gate driver to control a fully functional power converter based upon the half-bridge topology, a topology similar to the bidirectional DC/DC converter (BDC) found in EVs. The circuit accepts an input voltage from 36 V to 75 V and has an output voltage of 3.3 V with an output power up to 150 W. The circuit probing for each channel is as follows:

- Channel 1: switch node (yellow)
- Channel 2: HS gate V_{GS} (green)
- Channel 3: LS gate V_{GS} (orange)
- Channel 4: output voltage (blue)

The histograms show the collection of rise time (histogram 2) and fall time (histogram 3) data captured over time for both 0% and 65% loads. Note the near-Gaussian distribution of the rise time histogram and the asymmetrical distribution (trimodal) of the fall time histogram. The histograms for both rise and fall time change with different loads. Variations in rise and fall time are more easily visible with these diagrams for more detailed switching analysis. It is important to set the number of acquisitions in a run to the same number (e.g. 10000) to compare statistical data more easily.

Figure 10: Checking for overshoot and maximum voltage

(a) Low side V_{GS} with 0 % load

(b) Low side V_{GS} with 65 % load

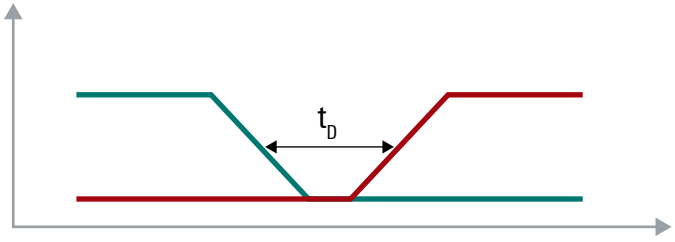
4 TESTING FOR RELIABILITY

Test coverage is the most important aspect in testing for reliability. Robust test checks must be performed for all corner cases to ensure that important design criteria are always met. Tests include load variation (particularly transient variations), input voltage variation (AC/DC converters do not have a constant input voltage), temperature variation and disturbances on the DC link (three-phase inverters with imbalances may cause disturbances). Another point to consider when testing for reliability is oscilloscope blind time; that is, the window of time between signal acquisitions when the instrument cannot perform a measurement. Most off-the-shelf oscilloscopes record only 90% of the time, making it difficult to capture transient situations. This is where a digital trigger really shows its value. As the oscilloscope captures data, the trigger is always enabled and works in real-time to ensure reliability. This is done by articulating design criteria as a trigger condition where multiple events can be stored in segmented memory, capturing the data for future analysis.

4.1 Trigger on a specific dead time

The following example of ensuring test reliability involves a scenario in which an EMI test fails for a design that is already complete. To pass the EMI test, the gate resistance can be increased, but this comes with a tradeoff: a change in rise time and possibly fall time as well. As shown in Figure 11, the changes in rise/fall time result in a change in dead time (t_D); that is, the delay between the HS and LS gate (or vice versa) at a certain voltage (e.g. threshold voltage). In this scenario, it is important to ensure that the circuit meets the minimum dead time requirements under all conditions (e.g. changes in temperature, VDC changes and load variations). The oscilloscope must be able to capture a potential violation on the minimal dead time, particularly for transient situations.

Figure 11: Dead time is the delay between the HS gate (red) and LS gate (green) at a certain voltage

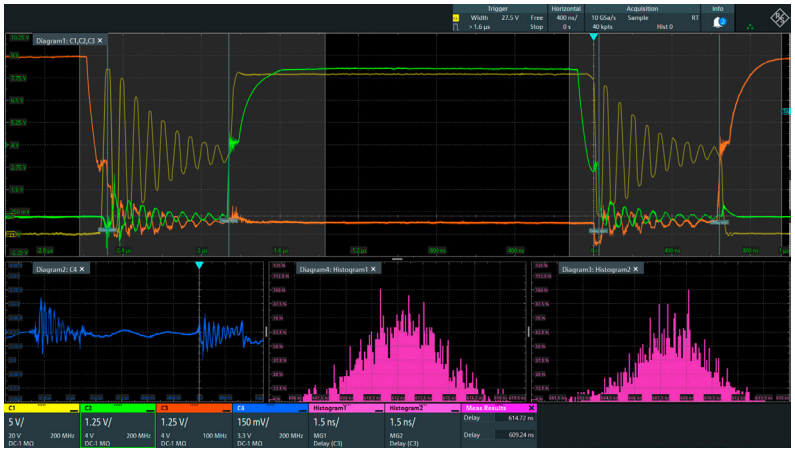


In order to do this without having to solder and re-solder various gate resistors, use a load transition and trigger on a specific dead time that is between the no load (0%) and high load (65%). The setup shown in Figure 12 is as follows:

- Channel 1: switch node (yellow)
- Channel 2: HS (green)
- Channel 3: LS (orange)
- Channel 4: output (blue)
- Histogram 1: LS switch (LS turning off and HS turning on)
- Histogram 2: HS switch (HS turning off and LS turning on)

Analysis of the no load (0%) shows a dead time between 608 ns and 611 ns with a variance of 2 ns. High load (65%) shows a dead time between 490 ns and 495 ns with a variance of 2 ns. The task then is to capture a load step (transient behavior) by looking for a dead time somewhere between 495 ns to 610 ns. Moving forward, the trigger will be set on a specific dead time between 510 ns and 540 ns.

Figure 12: Analyzing no load (0 %) scenario to assess dead time interval of the DUT



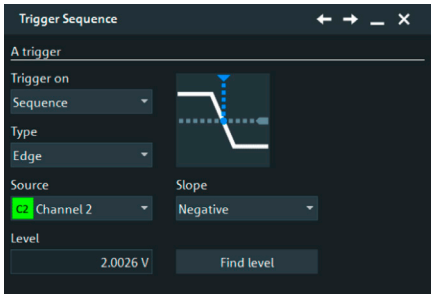
In order to trigger on a specific dead time, an A-B-R trigger (normal mode) can be set up (Figure 13) as follows:

- The A trigger event is set to the falling edge of channel 2
- The B trigger is set to the rising edge on channel 3 after 510 ns (the lower timing condition)
- The R (reset) is set after 540 ns

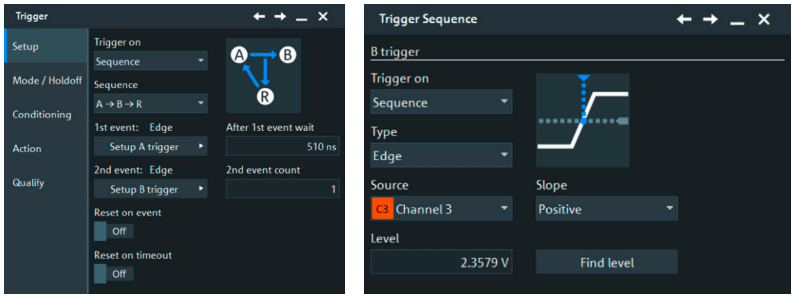
In other words, the entire trigger will reset after the upper timing condition. Both channel 2 and channel 3 thresholds are set below the threshold voltage (V_{th}). In this case, the trigger is set up to capture dead times between 510 ns and 540 ns. For example, if the dead time was 610 ns (not a violation of our minimum dead time) the trigger will not capture this event. For a minimum threshold, the B trigger can be set to 0 ns; this way, the trigger will capture any dead time below 540 ns. The key takeaway in this example is that trigger sensitivity relies on a complex timing definition.

Figure 13: Defining the A-B-R trigger

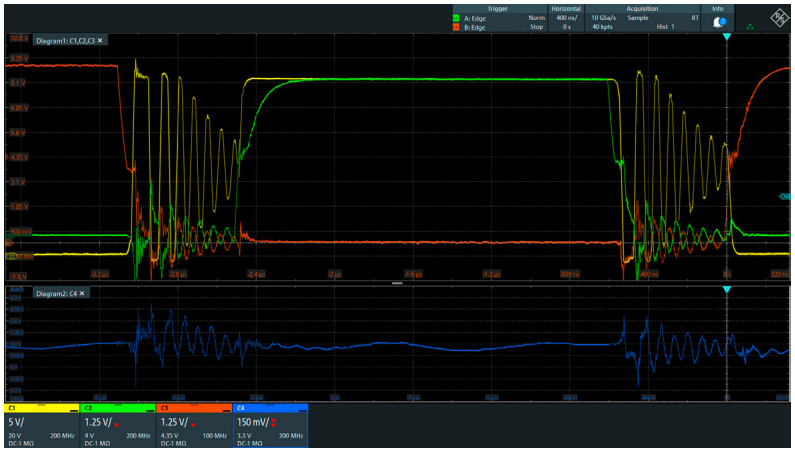
(a) The A trigger event is set to the falling edge of channel 2



(b) The B trigger event is set to the rising edge of channel 3 after 510 ns



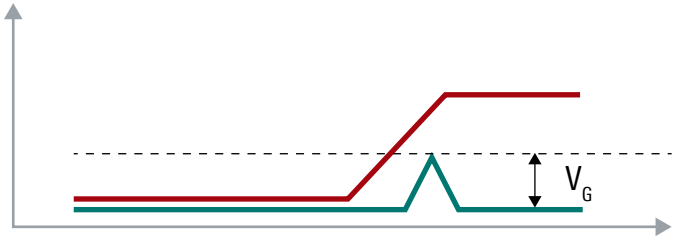
(c) Defining the A-B-R trigger



4.2 Trigger on high side V_{GS} glitch for no load

Another example of testing for reliability is in the design of a gate driver with a specified rise/fall time. Oftentimes, a glitch will appear on the HS switch that is induced by the turning on of the LS switch (Figure 14). The design criteria that requires testing in this scenario is the maximum tolerable glitch voltage (V_G) to avoid a shoot-through where the glitch opens up the HS transistor. This can be defined in more detail as the maximum tolerable V_G on the HS gate after the LS gate turns on. Testing this can be tricky because the glitch is typically load dependent and can also impact the gate driver output impedance and dead time.

Figure 14: A glitch voltage (V_G) will appear on the HS switch (green) when the LS switch (red) turns on



The probing can be set up as follows:

- Channel 1: switch node (yellow)
- Channel 2: HS channel (green)
- Channel 3: LS channel (orange)
- Channel 4: output (blue)

All channels have a bandwidth of less than 500 MHz so that high-definition (HD) mode can be turned on to increase to a 12-bit resolution. This offers users the ability to look for very low voltages and offsets — a necessity for triggering on a glitch. The A-B-R trigger (normal mode) is set up is as follows (see Figure 15):

- The A trigger event is set to the rising edge of channel 3
- The B trigger is set as a glitch trigger on high polarity with a length of 40 ns on channel 2 and is set to occur 5 ns after A trigger
- The R is set after 400 ns

The R trigger is set to avoid dead time, since glitches appear frequently during dead time. However, these will not cause the HS switch to turn on. The oscilloscope image in Figure 15 shows that the A trigger is set slightly below the threshold voltage and the B

trigger is set to the defined test voltage. With this setup, users can trigger right after the rising edge where the glitch on the high side appears.

Figure 15: Setting up the A-B-R trigger in normal mode to trigger on HS V_{GS} glitch with no load

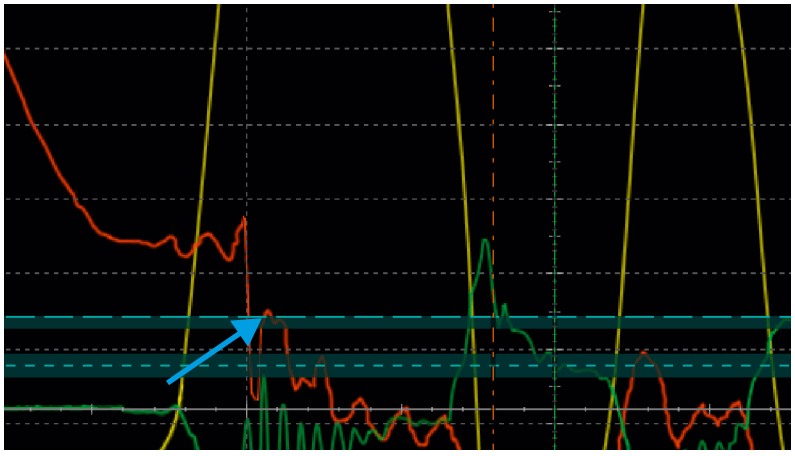
4.3 Trigger on high side V_{GS} glitch for high load

While the trigger settings in the previous section work well for no load, they fail when applying a high load (65 %), as shown in Figure 16.

Figure 16: Trigger misses a glitch event at high load

(a) The intended trigger point is missed (circled in blue). This is because there is a glitch on the B trigger but the A trigger captures a spike after a falling edge, during dead time.

(b) Magnification of the glitch on the B trigger



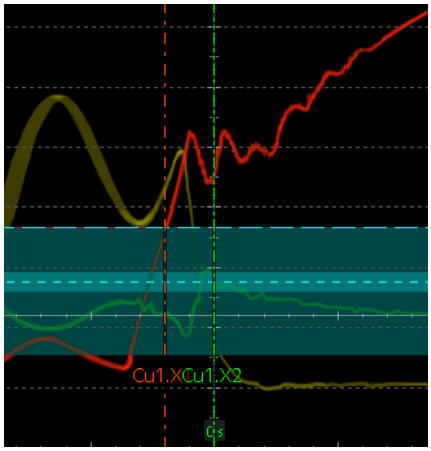
As shown in the figure, there is quite a bit of dead time, a quality often seen in bidirectional charger test setups. The resonance during the dead time shows glitches on both gate signals, resulting in a failure of the trigger to capture the time interval of concern. Raising the trigger level for channel 3 will not work in this instance because it violates the correlation in timing between channels 2 and 3.

The best way to resolve this issue is to increase the hysteresis of the A trigger so that it ignores spikes during resonance. The B trigger can be set right after LS gate turn on (20 ns via cursor movement) where the B trigger still maintains a small amount of hysteresis. The large A hysteresis and small B hysteresis can be seen in the magnification in Figure 17 where the oscilloscope is in "Run Continuous" mode over multiple acquisitions. The screenshot shows that the trigger condition is quite stable, capturing the right point in the waveform despite the complexities of DUT (e.g. load variations, resonances).

Figure 17: Oscilloscope in "Run Continuous" mode

(a) Oscilloscope in "Run Continuous" mode capturing thousands of waveforms at different loads while maintaining a very stable trigger to accurately capture the HS V_{GS} glitch condition

(b) Magnification



5 CONCLUSION

In order to test for power converter reliability, it is important to begin with the right test setup. The circuit must be carefully connected and account for voltage range, bandwidth and CMRR. When measuring the switch node and gate signal, use all available statistical information to gather valuable insights on the DUT.

Finally, articulating test criteria as a trigger condition greatly simplifies testing because it enables the oscilloscope to find violations in real-time. The digital trigger can be used to capture events that are otherwise very difficult to find. This allows engineers to change different parameters and test for highly specific events that could cause a failure. An oscilloscope that supports complex A-B-R trigger configurations, dedicated trigger hysteresis settings and complex target timing definitions is crucial to this process.

Rohde & Schwarz

The Rohde & Schwarz technology group is among the trailblazers when it comes to paving the way for a safer and connected world with its leading solutions in test & measurement, technology systems and networks & cybersecurity. Founded 90 years ago, the group is a reliable partner for industry and government customers around the globe. The independent company is headquartered in Munich, Germany and has an extensive sales and service network with locations in more than 70 countries.

www.rohde-schwarz.com

Rohde & Schwarz customer support

www.rohde-schwarz.com/support

PD 3685.0534.52 | Version 02.00 | September 2024 (ch) | White paper
Switching analysis
Data without tolerance limits is not binding | Subject to change